REMARKS

Claims 1-25 stand rejected under 35 U.S.C. §102(b) over *Patrick et al.*, U.S. Patent No. 5,706,483 (hereinafter *"Patrick"*). By this amendment, claims 2, 5, 9, 19, and 22 are corrected as to the Examiner's objection to informalities. In addition, while independent claims 1 and 11 are amended without adding any new matter, claims 8 and 18 are canceled without prejudice.

As amended, claim 1 calls for a method including writing transformed pixel data from a first memory location to a second memory location and transferring the pixel data to a memory controller using a memory controller client. These limitations of claim 1 may enable applying transformations, such as video and graphics transformations, without explicitly using a fetch engine resident in the physical memory. However, *Patrick* merely teaches a run-time code compiler for data block transfer by employing a state machine stored in the physical memory that transitions between a plurality of states from one transformation to another. See, column 6, lines 63-65; column 7, lines 44-49, and lines 65-67. Therefore, for at least this reason alone, independent claim 1 and the claims dependent thereon are not anticipated by the *Patrick* reference.

The Examiner states that the *Patrick* reference shows in Figure 1 the memory system 30 that controls relocating a pixel data in memory areas. In the *Patrick* reference, each of the states of the state machine contains a portion of code for fetching and writing of bytes. To perform a data block transfer, *Patrick* teaches a method for compiling a block of code from the code portions memory. In particular, a bit compiler compiles code from the initial state for aligning the next destination address with a word-aligned address in memory. See, column 8, lines 54-66.

Specifically, in the *Patrick* reference use of the state machine located at the physical memory may be required between transformations for fetching pixel data and/or parameters of the operation associated with the transformations from the physical memory or for writing back the transformed pixel data to the physical memory for each transformation. Based on the Examiner's assertion that the memory system 30 controls relocating the pixel data in memory areas combined with the teachings of the *Patrick* reference as set forth above, it can be safely

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presumed that the state machine in the memory is not required as an explicit fetch engine to be set up with the parameters of the operations associated with different transformations.

On the contrary, claim 1, as amended, does not involve the use of the memory controller for writing the transformed pixel data from a first memory location to a second memory location. An explicit fetch engine may not be required either to fetch pixel data or to set up the parameters of the operation associated with the transformations. In this manner, multiple transformations can be applied to the pixel data before transferring the transformed pixel data to the memory controller using a memory controller client.

Accordingly, the *Patrick* reference cannot anticipate claim 1 because the compiler taught by *Patrick* involves use of the state machine located at the physical memory between transformations, i.e., writing of transformed pixel data from one memory location to another memory location without depending upon the memory controller is not anticipated. Therefore, reconsideration of the rejection of independent claim 1 and the claims dependent therefrom is respectfully sought as these claims are in condition for allowance. Independent claim 11 calls for an article claim that corresponds to claim 1. For at least the reasons indicated above, claim 11 and the claims dependent therefrom cannot be anticipated by the *Patrick* reference.

With respect to claim 21, which is directed to a system including a memory controller that receives pixel data and addresses, a first memory controller client forwards pixel data and addresses to a first transfer function, and a second memory controller client receives data from the first transfer function together with the new addresses. There is not a remote hint whatsoever provided in the *Patrick* reference as to using two separate memory controller clients as claimed in claim 21.

All that the *Patrick* reference teaches is a method and apparatus for data block transfer using a run-time code compiler, which uses a state machine resident at the memory of a computer system. Use of two separate memory controller clients, one forwarding pixel data and addresses to a first transfer function and the second receiving the pixel data from the transfer function together with new addresses is absent from the *Patrick* reference. In this manner, the Applicant respectfully requests the Examiner that the §102 rejection of independent claim 21 is not adequate. Accordingly, the Examiner is requested to allow these claims. In addition, the

claims dependent from independent claim 21 are also patentably distinguishable over the *Patrick* reference since the cited reference fails to teach or suggest the Applicant's claimed invention of independent claim 21. The Examiner is respectfully requested to reconsider the pending claims.

Attached is an Appendix, which shows the changes to the claims. The Examiner is encouraged to review those changes to ensure that the claims, as set forth herein, correspond accurately to the claims in the appendix and no inadvertent errors have occurred.

In view of these remarks and amendments, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested.

Respectfully submitted,

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APPENDIX

1   1.   A method comprising:

2   writing pixel data to a first memory location;

3   performing a first pixel transformation at said first memory location;

4   generating a memory address for a second memory location; [and]

5   writing said transformed pixel data from said first memory location to said second

6   memory location[.]; and

7   <u>transferring said pixel data to a memory controller using a memory controller</u>

8   <u>client</u>.

1   2.   The method of claim 1 wherein writing pixel data to [a] <u>said</u> first memory

2   location includes writing pixel data to a first virtual memory location.

1   5.   The method of claim 1 wherein [entering an address] <u>generating said memory</u>

2   <u>address</u> for [a] <u>said</u> second memory location includes transforming the addresses of said pixel

3   data at said first memory location to addresses at said second memory location.

1   9.   The method of claim 1 wherein writing said transformed pixel data from said first

2   memory location to said second memory location includes writing said pixel data from [a] <u>said</u>

3   first memory location associated with a first transfer function to [a] <u>said</u> second memory location

4   associated with a second transfer function.

1   11.   An article comprising a medium storing instructions that enable a processor-based

2   system to:

3   write pixel data to a first memory location;

4   perform a first pixel transformation at said first memory location;

5   generate a memory address for a second memory location; [and]

6   write said transformed pixel data from said first memory location to said second

7   memory location[.]; and

8   <u>transfer said pixel data to a memory controller using a memory controller client.</u>

1   19.   The article of claim 11 further storing instructions that enable the processor-based

2   system to write said pixel data from [a] <u>said</u> first memory location associated with a first transfer

3   function to [a] <u>said</u> second memory location associated with a second transfer function.

1   22.   The system of claim 21 wherein said first <u>memory</u> controller client selectively

2   forwards pixel data and addresses to one of a plurality of transfer functions and said second

3   controller client receives pixel data with new addresses from [a] <u>said</u> plurality of transfer

4   functions.